WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

capacitor structures, each having a first lower electrode, a first insulating film formed on the first lower electrode and a first upper electrode formed on the first insulating film; and

electric fuse elements, each having a second lower electrode, a second insulating film formed on the second lower electrode and having an impurity concentration higher than that of the first insulating film, and a second upper electrode formed on the second insulating film, the electric fuse elements having substantially same structure as that of the capacitor structures and being formed on same level as that of the capacitor structures, wherein information is written in the electric fuse element depending on whether the second insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second insulating film which depends on the impurity concentration of the second insulating film.

2. A semiconductor device comprising:

capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and

electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein information is written in the electric fuse element depending on whether the second gate insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second gate insulating film which depends on the impurity concentration of the second gate insulating film.

3. The semiconductor device according to claim 2, further comprising an impurity diffusion layer of a second conductivity type, which is formed in at least a portion of the semiconductor substrate and which abuts on the second gate insulating film under the second gate electrode, the impurity diffusion layer being paired with the second gate electrode and serving as one electrode of the electric fuse element.

4. The semiconductor device according to claim 3, further comprising a leading electrode electrically connected to an extended portion of the impurity diffusion layer extending to a region of the semiconductor substrate where no second electrode exists.

5. The semiconductor device according to claim 2,

wherein the first gate insulating film and the first gate electrode constitute a part of a MOS transistor.

6. A method for fabricating an electric fuse comprising the steps of:

forming an insulating film on a first electrode;

forming a second electrode on the insulating film; and

injecting by ion injection an impurity into at least a portion of the insulating film or passing the impurity therethrough, thereby controlling dielectric breakdown resistance of the insulating film to set a writing voltage.

7. A method for fabricating a semiconductor device comprising the steps of:

forming a gate insulating film on first and second regions of a semiconductor substrate of a first conductivity type;

forming a first gate electrode layer on the gate insulating film; and

injecting by ion injection an impurity into a portion of the gate insulating film on the second region of the semiconductor substrate, thereby controlling dielectric breakdown resistance of the gate insulating film on the second region to set a writing voltage of an electric fuse comprising the second region of the semiconductor substrate, the gate insulating film located on the second region and

the portion of the first gate electrode layer on the second region.

8. The method according to claim 7, further comprising the steps of:

after the step of injecting the impurity into the gate insulating film, forming a second gate electrode layer on the first gate electrode layer; and

patterning the first and second gate electrode layers, thereby forming a gate electrodes of a MOS transistor on the first region of the semiconductor substrate and an electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first and second gate electrode layers on the second region.

9. The method according to claim 7, further comprising the steps of:

after the step of forming the first gate electrode layer, forming a second gate electrode layer on the first gate electrode layer; and

patterning the first and second gate electrode layers, thereby forming gate electrodes of MOS transistors on the first region of the semiconductor substrate, and electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first and second gate electrode layers on the second region.

10. The method according to claim 9, wherein

the step of injecting the impurity into the gate insulating film comprises the steps of:

injecting by ion injection an impurity of a second conductivity type into the gate insulating film located on the second region of the semiconductor substrate and into the second region of the semiconductor substrate that has been exposed by patterning the first and second gate electrode layers, thereby forming an impurity diffusion layer in a surface region of the semiconductor substrate; and

forming a leading electrode electrically connected to the impurity diffusion layer.

11. The method according to claim 10, wherein in the step of forming the impurity diffusion layer in the surface region of the semiconductor substrate, the impurity diffusion layer is also formed in a portion of the semiconductor substrate immediately under the first and second gate electrode layers located on the second region.

12. A method for fabricating a semiconductor device comprising the steps of:

forming a gate insulating film on first and second regions of a semiconductor substrate of a first conductivity type;

forming a first gate electrode layer on the gate insulating film; and

injecting an impurity into the second region of

the semiconductor substrate in contact with the gate insulating film by ion injection through the first gate electrode layer and the gate insulating film on the second region of the semiconductor substrate, thereby forming an impurity diffusion layer, controlling dielectric breakdown resistance of the gate insulating film on the second region to set a writing voltage of an electric fuse comprising the second region of the semiconductor substrate, the gate insulating film located on the second region and the first gate electrode layer located on the second region.

13. The method according to claim 12, further comprising the steps of:

after the step of injecting the impurity into the second region of the semiconductor substrate through the first gate electrode layer and the gate insulating film, forming a second gate electrode layer on the first gate electrode layer; and

patterning the first and second gate electrode layers, thereby forming gate electrodes of MOS transistors on the first region of the semiconductor substrate, and electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first and second gate electrode layers on the second region.

14. The method according to claim 13, wherein the step of patterning the first and second gate

electrode layers comprises the steps of:

removing the first and second gate electrode layers located on a portion of the second region of the semiconductor substrate, thereby exposing a surface of the impurity diffusion layer; and

forming a leading electrode electrically connected to the exposed impurity diffusion layer.

15. The method according to claim 12, further comprising the steps of:

after the step of forming the first gate electrode layer, forming a second gate electrode layer on the first gate electrode layer; and

patterning the first and second gate electrode layers, thereby forming gate electrodes of MOS transistors on the first region of the semiconductor substrate, and electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first and second gate electrode layers on the second region.

16. The method according to claim 15, wherein the step of injecting the impurity into the second region of the semiconductor substrate through the first gate electrode layer and the gate insulating film comprises the steps of:

injecting by ion injection an impurity of a second conductivity type into the semiconductor substrate in contact with the gate insulating film located under

the first and second gate electrode layers and into the second region of the semiconductor substrate that has been exposed by patterning the first and second gate electrode layers, thereby forming an impurity diffusion layer in a surface region of the semiconductor substrate; and

forming a leading electrode electrically connected to the impurity diffusion layer.

17. A method for fabricating a semiconductor device comprising the steps of:

forming a gate insulating film on first and second regions of a semiconductor substrate;

forming a first gate electrode layer on the gate insulating film;

patterning the first gate electrode layer, thereby forming gate electrodes of MOS transistors on the first region of the semiconductor substrate, and electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first gate electrode layer on the second region; and

injecting by ion injection an impurity from a direction obliquely with respect to a normal of the semiconductor substrate into a portion of the semiconductor substrate exposed by patterning the first gate electrode layer and a portion of the semiconductor substrate immediately under an edge portion of

the first gate electrode layer in the second region, thereby forming an impurity diffusion layer serving as one electrode of an electric fuse, the ion injection causing the impurity to pass through the gate insulating film or to be injected into the gate insulating film, thereby controlling dielectric breakdown resistance of the gate insulating film to set a writing voltage of the electric fuse.

18. The method according to claim 17, further comprising the step of, after the step of forming the first gate electrode layer, forming a second gate electrode layer on the first gate electrode layer.